IJAREEIE

e-ISSN: 2278-8875
p-ISSN: 2320-3765

International Journal of Advanced Research

in Electrical, Electronics and Instrumentation Engineering

Volume 10, Issue 3, March 2021

INTERNATIONAL STANDARD SERIAL NUMBER INDIA

Impact Factor: 7.122

| e-ISSN: 2278 – 8875, p-ISSN: 2320 – 3765| www.ijareeie.com | Impact Factor: 7.122|

||Volume 10, Issue 3, March 2021||

DOI:10.15662/IJAREEIE.2021.1003006

Decoding Logic for Vedic Arithmetic Computation

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ABSTRACT: Vedic Mathematics introduces the wonderful applications to Arithmetical computations theory of numbers, compound multiplications, algebraic operations, factorisations, simple quadratic and higher order equations, simultaneous quadratic equations, partial fractions, calculus, squaring, cubing, square root and cube root. This paper discusses the use of VLSI based computational logics for solving fundamental arithmetic computations which is useful in design of ALU circuitry with ASIC circuits.

KEYWORDS: Vedic Maths, DhwajankaSutra, Vedic Square Root

I. INTRODUCTION

Vedic Maths tricks, Addition, Subtraction, Multiplication & Division , is a system of reasoning and mathematical working based on ancient Indian teachings called Veda and it is fast, efficient, easy to learn [10]. Vedic mathematics, which simplifies arithmetic and algebraic operations, has increasingly found acceptance the world over. “Atharva Veda” is a scholarly Indian article which deals with the branches like Engineering, Mathematics, sculpture, Medicine, and all other sciences .The Sanskrit word Veda is derived from the root Vid, meaning to know without limit.

Vedic Mathematics introduces the wonderful applications to Arithmetical computations, theory of numbers, compound multiplications, algebraic operations, factorizations, simple quadratic and higher order equations, simultaneous quadratic equations, partial fractions, calculus, squaring, cubing, square root, cube root, coordinate geometry and wonderful Vedic Numerical code. Market available application specific ICs developed by leading manufacturers of microprocessors have developed their architectures to be suitable for conventional binary arithmetic methods. The need for faster processing speed is continuously driving major improvements in processor technologies, as well as the search for new algorithms

II. VEDIC ADDITION

Addition is the most basic operation, herein adding number 1 to the previous number generates all the numbers [10]. The Vedic Sutra describes that “By one more than the previous one describes the generation of numbers from unity.

1. Ten Point Circle

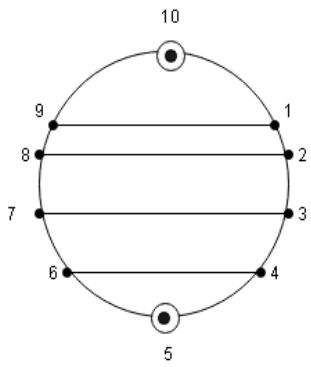

Figure1: Ten Point Circle

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||Volume 10, Issue 3, March 2021||

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[9+1; 8+2;7+3; 6+4; 5+5] sum-up to 10. These pair of numbers makes 10 on adding them.

2. Below a multiple of ten Rule can be used for adding a list of numbers

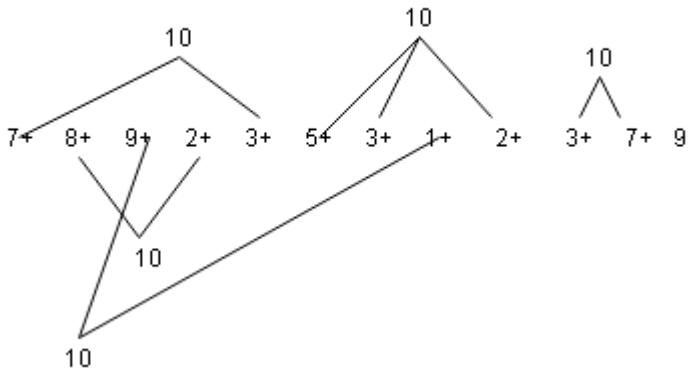

Figure2: Addition of list of numbers

Hence, 10+10+10+10+10+9=59.

III. VEDIC SUBTRACTION

Vedic Subtraction involves few simple rules to make subtrction easier[11].They are,
1.“ All from 9 and the Last from 10”Algorithm
Example:Subtract 789 from 1000 involves subtracting digits in the order that LSB is subtracted from 10 and the rest of digits through subtraction from 9s . So
7 8 9
↓ ↓ ↓ [Here all from 9 last from 10 means subtract 78 from 99 and 9 from 10, 211 is the solution].
2 1 1. Similarly ,considering from base number 10, 100, 1000 etc.Thus it makes Subtracting from a Base easier.

10000	from 100	from 100	from 100000
2772	54	97	10804
↓↓↓↓	↓↓	↓↓	↓↓↓↓↓
7228	46	03	89196

Example:1000 – 784 = 216

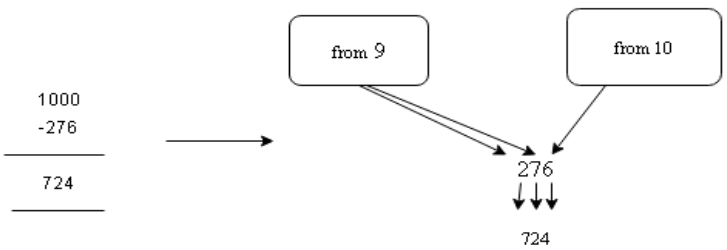

Figure 3: Vedic Rule is -All from 9 last from 10

IV. VEDIC MULTIPLICATION

Multiplication by a standard Algorithm is a general and efficient method to illustrate for a multiplication of a two digit numbers ,but this standard algorithm is hard when it is extended to more than two digits.Hence Vedic Multiplication plays an important role in its calculation[7,8].The Vedic method is based on the Urdhva-Tiryagbhyam

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sutra. The meaning of this sutra is that, it simply translates in English to say "vertically and crosswise". This Sutra is explained in the following steps.

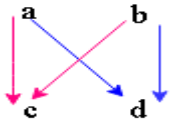

Figure 4: Vedic Multiplication

(a+b)*(c+d)=ad+bd+bc+ac

Urdhva-Tiryagbhyam Algorithm:

Step1. For the highest digit of the product, simply write the product of the highest digits of the 2 numbers.

Step 2. The process for the middle digits is a little tricky to explain using words. For each successive digit, you cross-multiply the highest digit of the top number by the next highest digit of the bottom number and the highest digit of the bottom number by the next highest digit of the top number

Step 3. Add these numbers together. This step is repeated for subsequent digits by decrementing the digit on the bottom number, cross-multiplying, incrementing the bottom digit while decrementing the top digit, and summing the products.

Step 4. For the lowest digit of the product, multiply the lowest digits of the numbers that is being multiplied.

Step 5. Throughout this process, only one digit can be kept per place, thus if the sum is higher than 9, then the ones digit alone is considered and implement a carry to the next higher place in the number.

Example: 341*562

Multiply the Ones Digit: 2*1 = 2

2)Multiplying the Tens Digit: 2*4+6*1 = 8+6 = 14 (write a 4, carry a 1)

3) Hundreds Digit: 2*3+4*6+5*1 = 6+24+5 = 35 (write a 5, carry a 3)

Note: At this point the end of the top number is reached, i.e. 2 cannot be multiplied by anything else, as there are no more digits. Thus, for the thousands digit we shall multiply 6 and 3 first, and then for the ten thousands digit, 5 and 3.

4) Thousands Digit: 6*3 + 5*4 = 18+20 = 38 (write an 8, carry a 3)

5) Ten Thousands Digit: 5*3 = 15 (the end of the multiplication is reached)

6) Add in the carries to produce the final answer, 191642

V. THE VEDIC DIVISION

Just as multiplication of counting numbers is based on repeated additions, the inverse operation of division may be understood in terms of repeated subtractions [4, 5]. In General, the division problem a ¸ b is the search for whole numbers q and r for whicha= b´q + r, where 0 < r < b. An efficient way of doing successive subtractions and solving for the numbers q and r is the long division algorithm. In Vedic Mathematics, the various methods used for division are

(i) Vilokanam sutra.
(ii) Nikhilam sutra—All from 9 and the last from 10.
(iii) Paravartya sutra—Transpose and Adjust.
(iv) Dhvajanka sutra—vertically and crosswise and on top of the flag.

Dhvajanka Sutra

Out of these methods, the most general method of division is 'vertically and crosswise and on top of the flag' [8]. This method is also called straight division. By this method, numbers of any size can be divided by numbers of any size. Before beginning with the method there are four names connected with division, they are, divisor, dividend, quotient and remainder. The divisor is the number that divides the dividend, the answer's in the quotient, the remainder's at the end. This method is explained with an example.

Example: Divide 7332 by 64

1. From the divisor 64, only the first digit i.e. 6 is written in division column

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2. Put the other digit i.e. 4 on top of the flag as shown alongside. As one digit is put on top of the flag, one place is allotted at the right end of the dividend to the remainder portion of the answer and make it off from the other digits by a vertical (dotted) line. The entire division is to be done by 6.
3. Divide 7 by 6 and get 1 as quotient and 1 as remainder, the first quotient digit 1 is written below the division line and prefix the remainder 1 up just before 3 (the next digit of dividend), to make gross dividend 13. From this, subtract the product of the flag digit 4 and the first digit of the quotient 1. Thus, (13 – (4 × 1)) = 9, which is the actual dividend.
4. Now (9 ÷ 6 = 1), remainder 3. Put quotient digit 1 and remainder 3 in the respective places as before. The next gross dividend is 33. From this, subtract the product of flag digit and the second quotient digit i.e. 4 × 1. Thus, [(33 – (4 × 1)) = 29], which is the next actual dividend.
5. Next, (29 ÷ 6 = 4) and remainder is 5. Put quotient digit 4 and remainder 5 in their respective places. The division is over and the gross remainder is 52. From this, subtract the product of the flag digit and the next digit of quotient i.e. (4 × 4). Thus, [(52 – (4 × 4)) = 36], which is the actual remainder. Hence, quotient is 114 and remainder is 36.

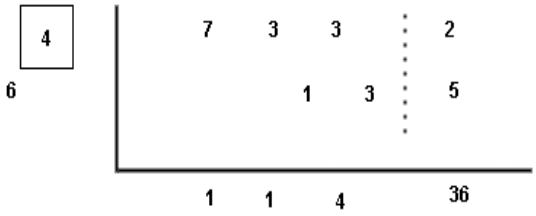

Figure 5 : Vedic Division by Dhwajanka sutra

Result:

Quotient is 114 and Remainder is 36.

"Vedic Mathematics" indicates the methodological operation and calculation based on ancient sutra and Upa-Sutras. These algorithms have been dedicated and extensively used for the faster manual calculation. Based on appreciation of these concepts, this paper proposes a new computation technique to determine Square Root of numbers. The proposed "Square Root Algorithm"is as below

Its Algorithm is explained below with a 4 digit number. Based on last digit various literals required are as presented below.

Table: Literals required for Computation of Square root.

Last Digit of the number	0	1	4	9	6	5
Last Digit of the Square number	0	1 or 9	2 or 8	3 or 7	4or 6	5

The Square root Algorithm is newly designed herein using the strategies used generally in Vedic arithmetic and is executed in two steps by finding out the unit digit and the last digit.

A. Finding the Unit Digit

Example: Solving '1296'

Step 1.Initially group the numbers the numbers as if pair, starting from the MSB & retain the LSB Bit only.

$$1_d 2_c 9_b 6_a$$

Step2: Considering the pair as dc=12

Obtain the perfect square, nearing 12 is '3'and 3*3=9.Hence the unit digit is '3'.

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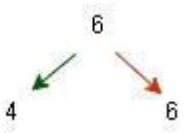
B.Finding the LSB Digit:

Step 3: Looking at the LSB digit 'a ', the possibilities of 'a' is,



Step 4:
In order to determine the possibilities, a small calculation is done on result of step2,

e= [Unit digit * (unit digit +1)]

Hence e=3*4
e=12
If 'e' is less then the least possibility literal is considered.
If 'e' is ≥ dc then the greater possibility is taken into account.
Hence the result of computation is from e, a. Thus

√1296 = 36

VI. DISCUSSIONS BASED ON VLSI LOGIC

This section of the paper presents the computation algorithm designed using Verilog Hardware Description Language and behavioural form of coding applied to various Vedic computation sequences like finding the Addition, Subtraction, Multiplication, Division and Square root of numbers.The functionality, design and analysis is carried out for 32-bit input. It is simulated using Xilinx ISim simulator synthesized using Xilinx XST for SPARTAN 6 family XC6SLX25T device with the speed -3 and package FGG484 FPGA. The operation and working is verified for the given set of inputswith results generated fromthe Verilog HDL test bench.

Addition Output:

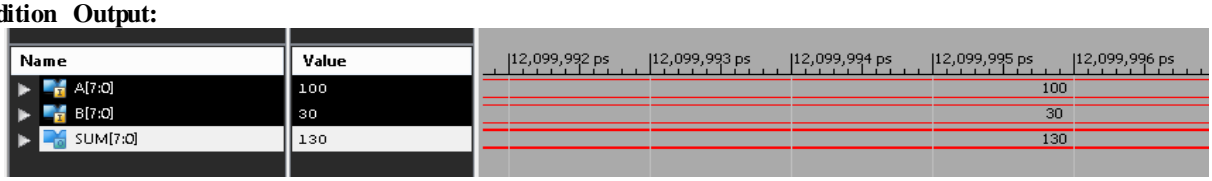


Figure 6a:Vedic Addition

Inference: [Input: A=100B=30Output: Sum=130]

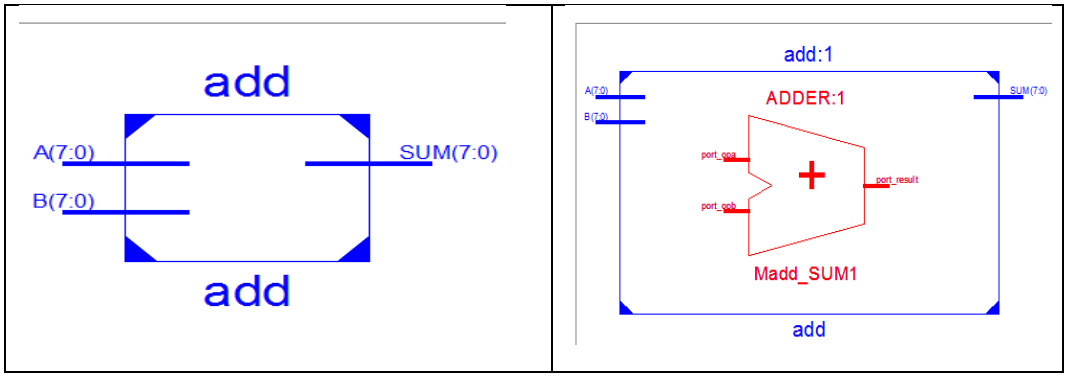


Figure 6b: RTL Schematic for Vedic Addition

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Subtraction Output:

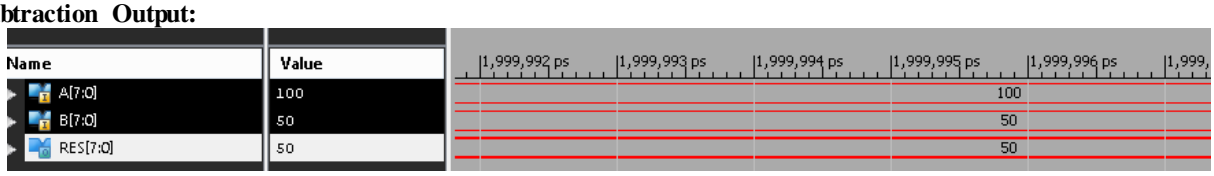

Figure 7a:Vedic Subtraction

Inference: [Input: A=100 B=50 Output: Res =50]

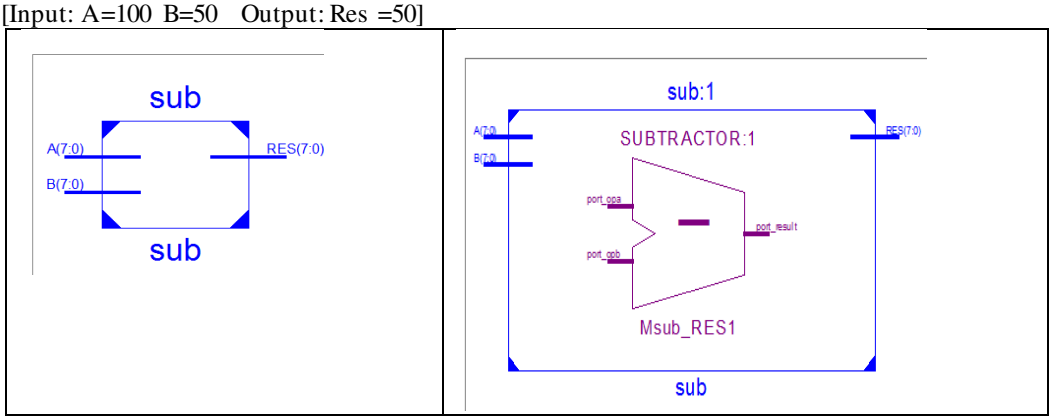

Figure 7b: RTL Schematic for Vedic Sub tractor

Multiplication Output:

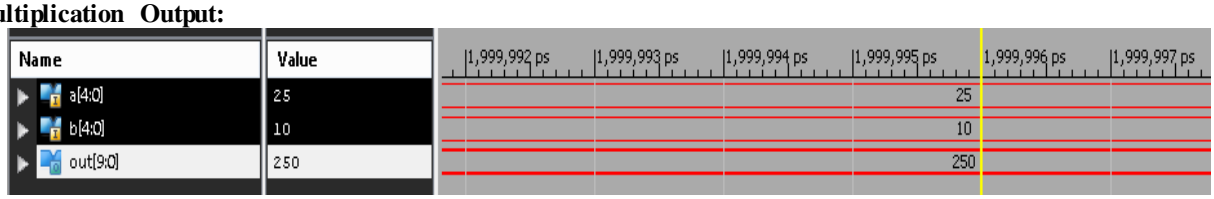

Figure 8 a: Vedic multiplication

Inference:Input: [a=25 b=10] Output: [Out=250]

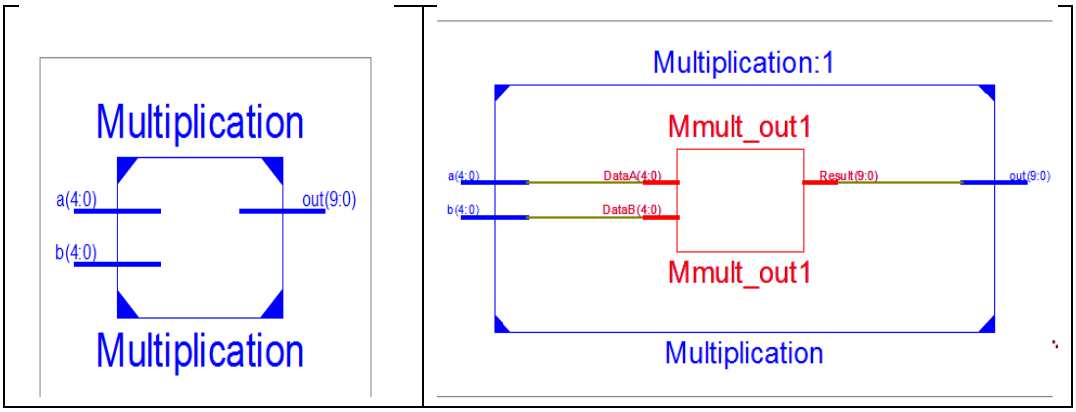

Figure 8b: RTL schematic fora Vedic Multiplier

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Division output:

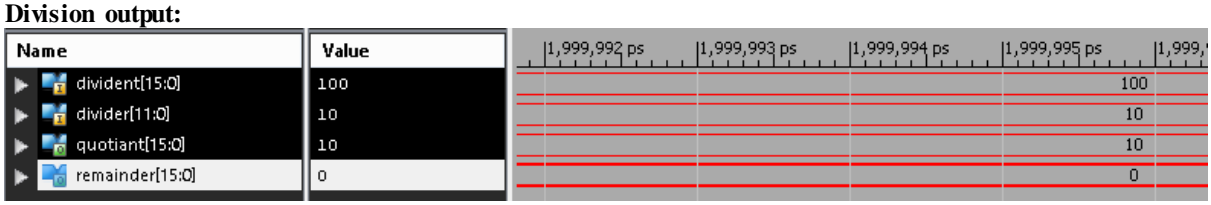

Figure 9a: Vedic Division

Inference: [Dividend =100 Divisor=10 Quotient=10 Remainder=0]

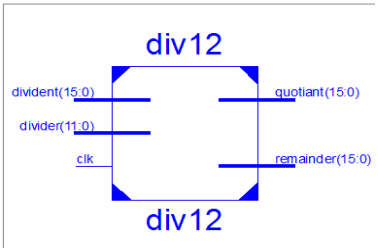

Figure9b: RTL Schematic for a Vedic Division

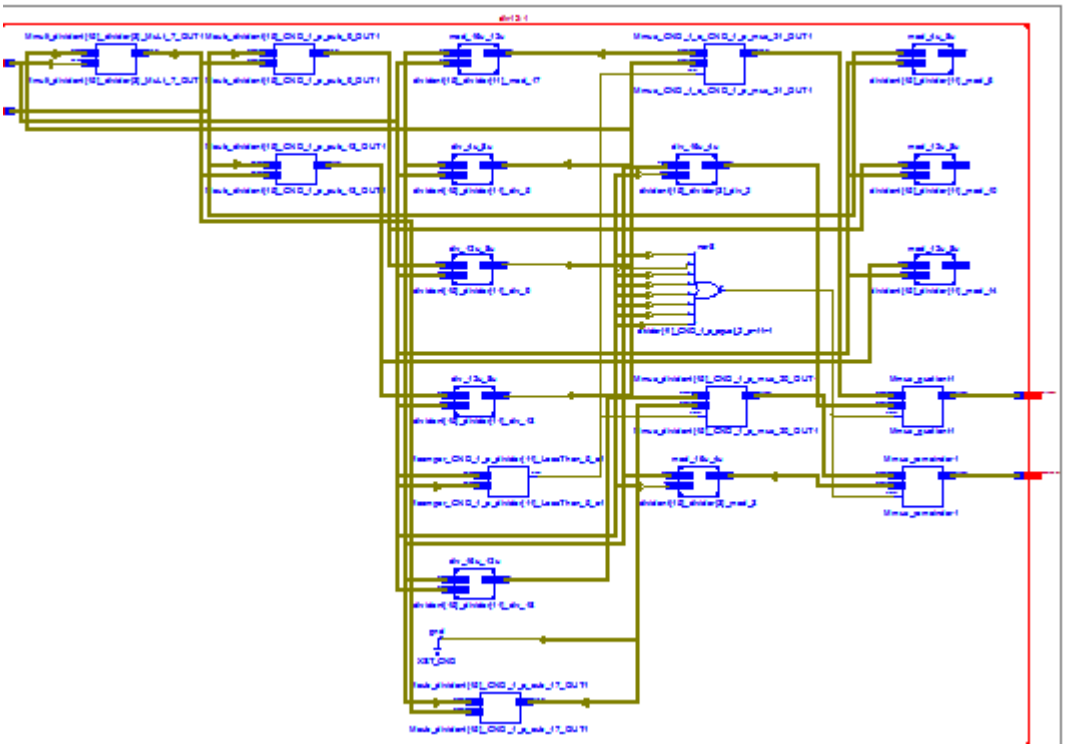

Figure 9c: RTL Schematic for a Vedic Division

Square Rootcomputation: Many engineering computations demand the evaluation of square root, for which the Vedic sutra is not available in Literature. The results shown herein is a new contribution since the logical steps in evaluation of square root is discussed with also including the corresponding Verilog designfor evolving its RTL Schematic realisable in a VLSI chip.

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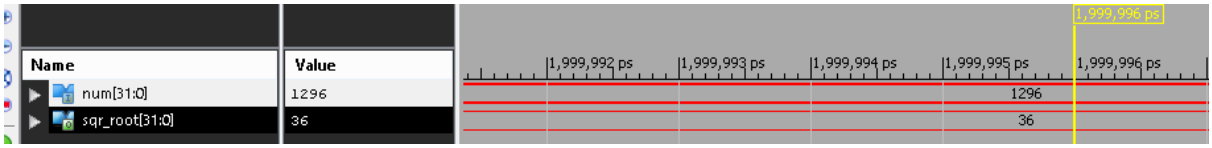

Figure 10a: Simulation Result of a Square root by Vedic Method

Inference:[Number: 1296 Square root of the number: 36]

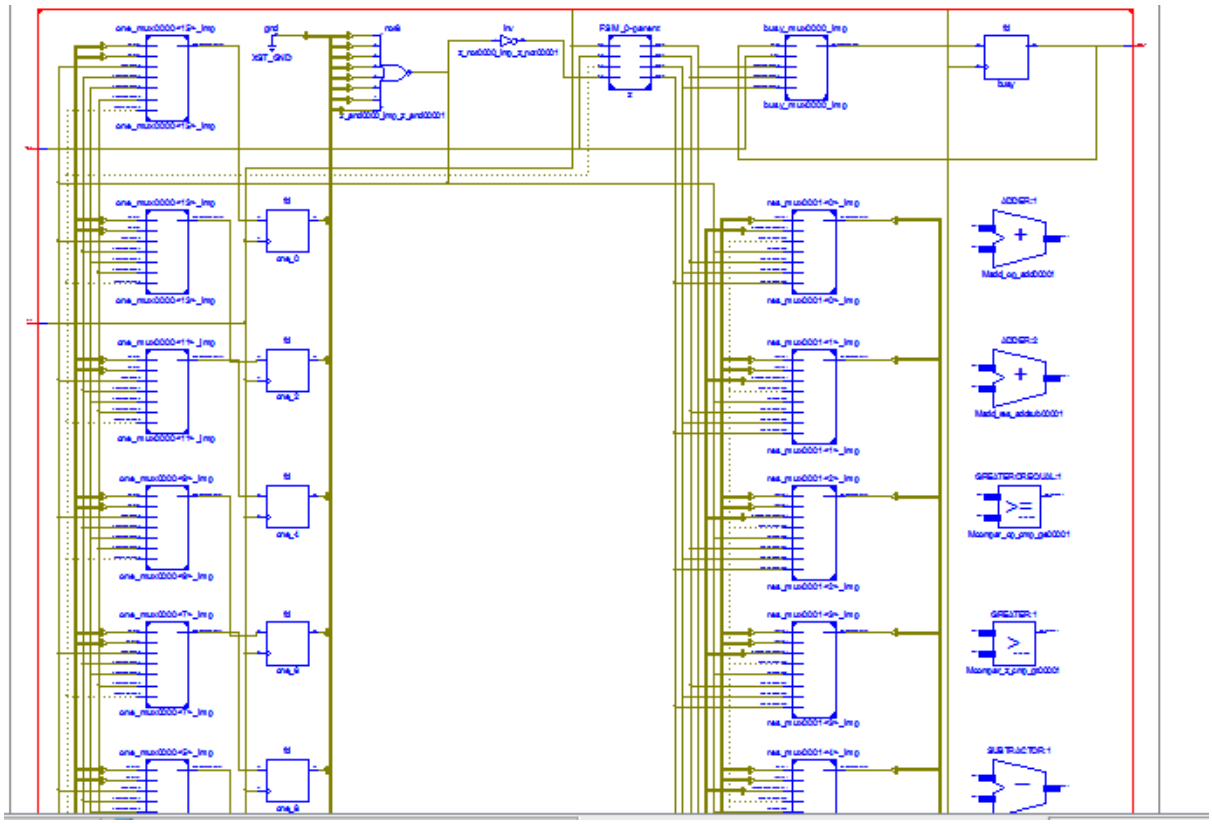

Figure 10b: RTL schematic for Vedic Square Root computation

TABLE 2: Device Summary:

Arithmatic Algorithm using VedicComputation	**DEVICE UTILISATION inVLSI forArithmetic Algorithm using Vedic Computation**
Addition:	Device Utilization Summary (estimated values) [-]

Logic Utilization	Used	Available	Utilization
Number of Slices	4	4656	0%
Number of 4 input LUTs	8	9312	0%
Number of bonded IOBs	24	66	36%

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Subtraction:

Logic Utilization	Used	Available	Utilization
Number of Slices	4	4656	0%
Number of 4 input LUTs	8	9312	0%
Number of bonded IOBs	24	66	36%

Multiplication:

Device Utilization Summary (estimated values)			[-]
Logic Utilization	**Used**	**Available**	**Utilization**
Number of Slice LUTs	33	63400	0%
Number of fully used LUT-FF pairs	0	33	0%
Number of bonded IOBs	20	210	9%

Division:

Device Utilization Summary (estimated values)			[-]
Logic Utilization	**Used**	**Available**	**Utilization**
Number of Slice LUTs	1929	63400	3%
Number of fully used LUT-FF pairs	0	1929	0%
Number of bonded IOBs	60	210	28%

Square root:

Device Utilization Summary (estimated values)			[-]
Logic Utilization	**Used**	**Available**	**Utilization**
Number of Slices	87	4656	1%
Number of Slice Flip Flops	43	9312	0%
Number of 4 input LUTs	163	9312	1%
Number of bonded IOBs	27	66	40%

VII. CONCLUSION AND FUTURE WORK

As illustrated in the results, the Vedic Arithmetic computations is observed to be capable for significantly reducing the area that improves the speed of computation. From the device Summary of various Arithmetic Operations using Vedic method presented in Table2, the methodology discussed in this paper is beneficial, as it greatly reduces the number of LUTs and the number of Input Output Blocks. It is bewitching to see the exploitation in the present VLSI technology for the faster execution in recent times.The design can be used toconfigure efficient architecture for various arithmetic circuits applicable to processes whereinthe arithmetic operations are exclusively performed. The algorithm for **Square root computation based on Vedic maths is newly proposed** through this paper**.** Design of ICs based on VLSI would be effective for the future ICs that demand high speed computations involving reduced micro steps. The future work is a proposal to develop an advanced shifter and adder/sub-tractor logical unit which can be infused to further improve the efficiency and performance of the arithmetic operations. Experimental implementation onto Application specific Integrated Circuit for the arithmetic operations is to be incorporated to validate the power efficiency of these circuits to gain overall efficiency of the system.

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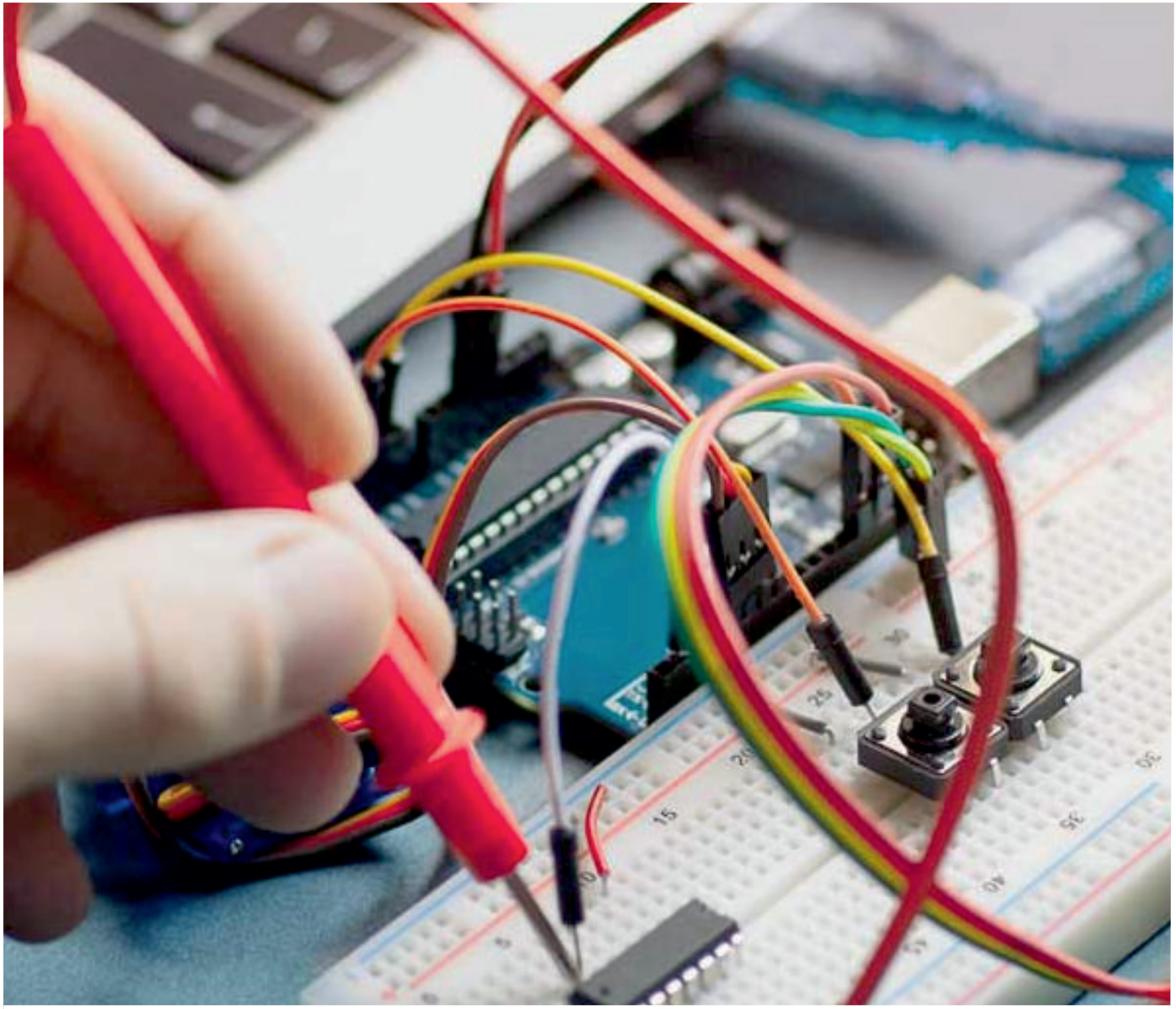

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